REMARKS

Claims 1-5, 13-17, and 25-29, all the claims pending in the application, stand rejected on prior art grounds. Applicants respectfully traverse these rejections based on the following discussion.

I. The Prior Art Rejections

Claims 1-5, 13-17, and 25-19 stand rejected under 35 U.S.C. §103(a) as being unpatentable over Salling et al. (U.S. Publication No. 2004/0114287), hereinafter referred to as Salling, in view of Kishida et al. (U.S. Publication No. 2001/0053948), hereinafter referred to as Kishida. Applicants respectfully traverse these rejections based on the following discussion.

The claimed invention provides a methodology for displaying a ring guard within an integrated circuit design. In the rejection, the Office Action argues that Salling discloses a method of displaying at least one guard ring within a hierarchical integrated circuit design. In addition, the Office Action argues that Salling and Kishida disclose a method of displaying a parameter symbol. However, neither Salling nor Kishida disclose a method of displaying a guard ring within a hierarchical integrated circuit design, comprising displaying a parameterized symbol. Instead, Salling discloses a hierarchy of guard rings, but NOT a hierarchy of integrated circuitry. Moreover, nothing in Salling nor Kishida disclose parameterized symbols or the display of any type of symbol(s). Therefore, as explained in greater detail below, Applicants respectfully submit that the prior art of record does not teach or suggest the claimed invention.

The Office Action asserts that Salling teaches a method of displaying at least one guard ring within a hierarchical integrated circuit design (pg. 5, § 10, ¶ 1). Citing Figure 3 of Salling, the Office Action goes on to reference first guard ring 110, second guard ring 120 and third guard ring 310 as system components which evidence a "hierarchical *integrated circuit*" (pg. 5, § 10, ¶ 1 (emphasis added)). Applicants respectfully disagree with such a conclusion, and assert that such system components provide a hierarchy of guard rings and NOT a hierarchy of integrated circuitry.

More specifically, Salling provides a first guard ring 110 for biasing the substrate when an ESD pulse is being discharged (pg. 2, ¶ 25, ll. 1-10). Moreover, Salling provides a second guard ring 120 for providing uniformity of the substrate bias (pg. 1, ¶ 9, ll. 11-15); and a third guard ring 130 for reducing the switching noise in the substrate (pg. 4, ¶43, ll. 5-8). Thus, Salling discloses system components which establish a hierarchy of guard rings. However, contrary to Applicants' invention, nothing in Salling discloses displaying guard ring(s) within a hierarchical integrated circuit design.

As described on page 8, paragraph 2 of Applicants' disclosure, circuits can change in circuit topology as well as physical space in the graphical representation. As a result, a guard ring needs to be able to expand with the growth of the hierarchical parameterized cell (P-cell). Furthermore, as described on page 13, paragraphs 2-3 of Applicant's disclosure, Figure 7 is a graphical illustration of an input node ESD P-cell that can be used in a hierarchical design. This P-cell includes voltage lines VDD 70 and VSS 72 P+/N- well diodes 71 that are positioned between the stretch lines 73. This P-cell can be auto-generated and actually contains two primitive parameterized (twin diodes). Figure 8

illustrates the same structure as that shown in Figure 7 and includes the guard ring 80. In this implementation, the new P-cell is modified in that it is now contain all the data information of the parameterized cell guard ring as well as the ESD P-cell.

Additionally, the relative placement (spacing) of the two P-cells (the input node ESD P-cell and the guard ring P-cell) will allow evaluation of the parasitic elements formed between the first and second P-cells. For example, a lateral npn can be formed between the ESD P-cell well, and the guard ring (if of n-type dopant). This parasitic npn can be represented as an additional circuit element within the hierarchical P-cell and can be used to evaluate the injection to the guard ring P-cell and its effectiveness in absorbing electrical current. In this fashion, the guard ring efficiency can be evaluated based on its effectiveness in collecting and absorbing electrical transient currents, noise injection, and other latchup inducing sources of current. This information can be stored in the higher hierarchical P-cell information for evaluation of latchup sensitivity from internal or external sources. Hence, the integration of the first and second parameterized cells (the input node ESD P-cell and the guard ring P-cell) leads to the ability to evaluate latchup, guard ring efficiency, and the interaction between the first ESD P-cell and its adjacent guard ring. In this fashion, circuit simulation can be performed and latchup sensitivity can be evaluated as a result of the P-cell circuit schematic cell view that contains the parasitic information.

Therefore, contrary to the position taken in the Office Action, Applicants submit that Salling does not teach or suggest a method of displaying at least one guard ring within a hierarchical integrated circuit design. Thus, it is Applicants' position that Salling

does not disclose or suggest the claimed feature of "displaying a guard ring within an integrated circuit design" as defined by independent claim 13.

In addition, the Office Action asserts that Salling teaches a method of displaying a parameter symbol (pg. 6, § 11, ¶ 2). To support this conclusion, the Office Action highlights, on page 6, section 11, paragraph 2, Salling's ability to utilize different types of circuitry (Salling, pg. 4, claim 7) and different types of guard rings (Salling, pg. 4, ¶ 40, ll. 15-19; ¶ 42, ll. 1-3; and ¶ 43, ll. 1-9). Further, the Office Action discusses the effectiveness of Salling's circuitry (Salling, pg. 4, claim 6). However, contrary to the position taken in the Office Action, none of the foregoing discloses displaying a parameterized symbol. Moreover, nothing in Salling discloses parameterized symbols or the display of any type of symbol(s).

Unlike Salling, Applicant's disclosure teaches displaying a parameterized symbol. As described on page 5, paragraph 4 of Applicant's disclosure, the symbolic display comprises a parameterized symbol. The parameterized symbol displays parameters including the type of circuit, the type of guard ring and the efficiency of the guard ring.

The Office Action also asserts that Kishida teaches a method of displaying a parameter symbol (pg. 6, § 11, ¶ 2). However, the Office Action does not refer to the specification, figures or the claims of the Kishida application to support this conclusion. Applicants respectfully submit that unlike Applicants' invention, nothing in Kishida discloses displaying a parameterized symbol. Moreover, nothing in Kishida discloses parameterized symbols or the display of any type of symbol(s).

Therefore, contrary to the position taken in the Office Action, Applicants submit that neither Salling nor Kishida, either individually or in combination, teaches or suggests a method of displaying a parameter symbol. Thus, it is Applicants' position that neither Salling nor Kishida, either individually or in combination, teaches or suggests the claimed feature of "displaying a parameterized symbol" as defined by independent claims 1, 13 and 25.

II. Formal Matters and Conclusion

With respect to the objection/rejections to the claims, the claims have been amended, above, to overcome these objection/rejections. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the objection/rejections to the claims.

Thus, as shown above, Salling does not disclose or suggest the claimed feature of "displaying a guard ring within an integrated circuit design" as defined by independent claim 13. Further, neither Salling nor Kishida, either individually or in combination, teaches or suggests the claimed feature of "displaying a parameterized symbol" as defined by independent claims 1, 13 and 25. Therefore, it is Applicant's position that the proposed combination of Salling and Kishida does not teach or suggest many features defined by independent claims 1, 13 and 25 and that such claims are patentable over the prior art of record. Further, it is Applicant's position that dependent claims 3-5, 15-17, and 27-29 are similarly patentable, not only because of their dependency from patentable independent claims, but also because of the additional features of the invention they

defined. In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw this rejection.

Accordingly, Applicants submit that claims 1, 3-5, 13, 15-17, 25 and 27-29 are patentably distinct from the prior art of record and are in condition for allowance. The Examiner is respectfully requested to pass the above application to issue at the earliest possible time. Should the Examiner find the application to be other than in condition for allowance, the Examiner is requested to contact the undersigned at the local telephone number listed below to discuss any other changes deemed necessary.

Respectfully submitted,

Dated: 9/21/05

Duane N. Moore, Esq.
Registration No. 53,352

McGinn & Gibb, P.L.L.C.
2568-A Riva Road, Suite 304
Annapolis, MD 21401
(410) 573-1123
Customer Number: 29154